8) The circuit below is most likely $\qquad$ -

9) A device that is used to switch one of several input lines to a single output line is called a $\begin{array}{llll}\text { A) multiplexer } & \text { B) demultiplexer } & \text { C) decoder } & \text { D) comparator }\end{array}$
10) If the data select lines of the MUX are $S_{1} S_{0}=11$, the output will be $\qquad$

C) HIGH
D) LOW
11) What distinguishes the look-ahead-carry adder?
A) It is easier to implement logically than a full-adder
A) It is easier to implement logically than a
B) It is slower than the ripple-carry adder.
B) It is slower than the ripple-carry adde
C) It is faster than a ripple-carry adder.
C) It requires advance knowledge of the final answer.


Figure 6-3
12) The output of the decoder in Figure 6-3 will be 1 only when $\qquad$ .
B) $\mathrm{A}=1, \mathrm{~B}=1, \mathrm{C}=1, \mathrm{D}=1$
$\qquad$
A) $\mathrm{A}=0, \mathrm{~B}=1, \mathrm{C}=0, \mathrm{D}=1$
C) $\mathrm{A}=0, \mathrm{~B}=0, \mathrm{C}=0, \mathrm{D}=0$
D) $\mathrm{A}=1, \mathrm{~B}=0, \mathrm{C}=1, \mathrm{D}=0$
$\qquad$

1) The carry output of a half-adder circuit can be expressed a $\qquad$ ) None of these
2) $\qquad$
3) $\qquad$
) The expression $A \oplus B$ represents
B) The summing output of a full-adder D) The carry output of a half-adder


Figure 6-1
3) The symbol in Figure 6-1 represents a(n) C) Half-adder
D) Full-adder
3) $\qquad$

