Digital Design Laboratory

Dr. Oniga István University of Debrecen, Faculty of Informatics

This work was supported by the construction EFOP-3.4.3-16-2016-00021. The project was supported by the European Union, co-financed by the European Social Fund.

9. Laboratory assignments

- Clock divider
- 8-bit synchronous up counter with asynchronous clear with LED output
- 8-bit counter with 7 segment display

1. Design and implement a clock divider circuit with two outputs: one having a frequency around 1 Hz and second around 100 Hz. Test the circuit on board with the two outputs connected to LED 1 and LED 15.

- 2. Add an 8-bit counter to the previous design and connect the two modules in a top module. The top module could designed in Verilog or schematic.
- 3. Add the hex7seg module and connect in a top module the 3 modules added to the project.

