Digital design laboratory (INSK220L)

**LABORATORY REPORT Digital design laboratory (INSK220L)**

**Laboratory assignments checklist**

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| Laboratory cod: | Date: |
|  |  |
| Students name: | NEPTUN code: |
|  |  |
| Supervisor name: | Result: |
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|  | 1. **Laboratory assignments**
 | Mandatory / Optional | Source files[pcs] | .bit file[1/0] | Report Questionnaire[1/0] | Date | Result |
| Lab1\_1 | 2 variable logic function implementation - schematic design | M |  |  |  |  |  |
| Lab1\_2 | 2 variable logic function implementation - HDL design entry | M |  |  |  |  |  |
| Lab1\_3 | command 8 LEDs using 8 switches on the board - HDL design entry | O |  |  |  |  |  |
|  | 1. **Laboratory assignments**
 |  |  |  |  |  |  |
| Lab2\_1a | 3 variable logic function implementation - Associative rules | M |  |  |  |  |  |
| Lab2\_1b | 3 variable logic function implementation - Distributive rules | - |  |  |  |  |  |
| Lab2\_1c | 3 variable logic function implementation - Absorption rules | - |  |  |  |  |  |
| Lab2\_2a | De Morgan rules for 2 variables | M |  |  |  |  |  |
| Lab2\_2b | De Morgan rules for 3 variables | O |  |  |  |  |  |
| Lab2\_2c | De Morgan generalization (optional assignment) | O |  |  |  |  |  |
| Lab2\_3a | AND, OR, XOR and NOR functions simulation and implementation | M2 |  |  |  |  |  |
|  | 1. **Laboratory assignments**
 |  |  |  |  |  |  |
| Lab3\_1 | Two level logic implementation - XOR function implementation | M |  |  |  |  |  |
| Lab3\_2 | BCD – 7 segments decoder „a” segment  | M |  |  |  |  |  |
| Lab3\_3 | 7 segment display | M |  |  |  |  |  |
|  | 1. **Laboratory assignments**
 |  |  |  |  |  |  |
| Lab4\_1a | Decimal to BCD encoder structural description | M |  |  |  |  |  |
| Lab4\_1b | 8 to 3 encoder structural description. Simulation and implementation. | O2 |  |  |  |  |  |
| Lab4\_1c | Priority encoder behavioral description with if | O |  |  |  |  |  |
| Lab4\_2a | Binary decoder from 3 to 8 - Structural description | O |  |  |  |  |  |
| Lab4\_2b | Binary decoder from 3 to 8 - Behavioral description | M |  |  |  |  |  |
| Lab4\_3a | 2:1 multiplexer - Behavioral description | O |  |  |  |  |  |
| Lab4\_3b | 4:1 multiplexer - Structural description | O |  |  |  |  |  |
| Lab4\_3c | 4:1 multiplexer - Behavioral description | M |  |  |  |  |  |
| Lab4\_3d | Generic multiplexer - Behavioral description | O |  |  |  |  |  |
|  | 1. **Laboratory assignments**
 |  |  |  |  |  |  |
| Lab5\_1a | Comparators for 2-bits numbers | M |  |  |  |  |  |
| Lab5\_2 | Parity generator | O2 |  |  |  |  |  |
| Lab5\_3a | 1-bit half adder simulation | M |  |  |  |  |  |
| Lab5\_3b | 1-bit full adder (using 2 half adders) implementation | M |  |  |  |  |  |
| Lab5\_4 | 1-bit full adder behavioral | M |  |  |  |  |  |
| Lab5\_5a | 4-bits adder structural description | O |  |  |  |  |  |
| Lab5\_5b | 4-bits adder behavioral description | M |  |  |  |  |  |
|  | 1. Laboratory assignments
 |  |  |  |  |  |  |
| Lab6\_1a | 4-bits subtractor | O |  |  |  |  |  |
| Lab6\_2 | 1 bit ALU | O |  |  |  |  |  |
| Lab6\_3 | 4-bits ALU | M |  |  |  |  |  |
| Lab6\_3b | 4-bits ALU – simulation | O |  |  |  |  |  |
| Lab6\_4 | 4-bits ALU result display on 7segments | M |  |  |  |  |  |
|  | 1. Laboratory assignments
 |  |  |  |  |  |  |
| Lab7\_1a | D-latch | M |  |  |  |  |  |
| Lab7\_1b | D flip-flop (rising edge of clock) | M |  |  |  |  |  |
| Lab7\_1c | D flip-flop (fallinf edge of clock) | O |  |  |  |  |  |
| Lab7\_2 | Flip-Flopok (a-d, 1 from 4) | M |  |  |  |  |  |
| Lab7\_3 | T-FF (a or b) | M |  |  |  |  |  |
|  | 1. Laboratory assignments
 |  |  |  |  |  |  |
| Lab8\_1a | 4-bit synchronous up counter with asynchronous clear | M |  |  |  |  |  |
| Lab8\_1b | 4-bit synchronous up counter with synchronous clear | O |  |  |  |  |  |
| Lab8\_2 | 4-bit synchronous down counter with synchronous clear | O |  |  |  |  |  |
| Lab8\_3 | 4-bit synchronous up/down counter | O |  |  |  |  |  |
| Lab8\_4 | Decimal up counter with load | M |  |  |  |  |  |
| Lab8\_5 | N-bit synchronous up counter with asynchronous clear | M |  |  |  |  |  |
| Lab8\_6 | Clock divider | M |  |  |  |  |  |
| Lab8\_7 | 8-bit counter with LED output | M |  |  |  |  |  |
| Lab8\_8 | 8-bit counter with 7 segment display | M |  |  |  |  |  |