UNIVERSITY of DEBRECEN

Dr. József Sütő
Department of IT Systems and Networks

Evaluation Sheet

Programmable Logical Devices

Lab 1

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
Simulation – 200ns	8	2			
Extended Simulation	10	2			
Program the FPGA	13	2			

Lab 2

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
2:1 MUX	1	1			
2-bit 2:1 MUX	2	1			
Connect switches	3	1			
2-bit 2:1 MUX simulation	4	1			
2:1 MUX behavioral	5	1			
3:1 MUX	6	2			

Lab 3

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
3-8 decoder	1	2			
74138 decoder	2	2			
7-seg decoder	3	2			
8-3 encoder	4	2			

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Lab 4

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
4-bit number on 7-segment disp.	1	2			
2-out-of-5 code	2	2			
4-bit number on 7-seg and led	3	4			

Lab 5

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
comparator with ROM	1	2			
multiplier with ROM	2	2			
simple ROM	3	2			

Lab 6

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
add two values task	1	1			
even parity task	2	2			
add two values function	3	1			
calculate ones function	4	2			
waveform generator	5	2			

Lab 7

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
inter delay sim.	1	2			
intra delay sim.	2	2			
BCD-Gray converter	3	2			

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Lab 8

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
1s pulse	1	2			
BCD visualizer	2	3			
4-bit counter	3	2			

Lab 9

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
Traffic light	1	1			
1Hz traffic light	2	2			
Bit sequence detector	3	3			

Lab 10

Exercises	Section	Point	1. student's Neptun code	2. student' s Neptun code	…
Multiplier ASM chart	1	3			
Multiplier simulation	2	3			